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**Title: Intellera: A Hardware-Based Acceleration of Matrix MAC Processor**

**Problem Statement:**

In the field of machine learning, matrix multiplication is a fundamental operation that plays a crucial role in various algorithms and computations. However, traditional processors often struggle to efficiently execute matrix multiplication tasks due to their general-purpose nature. This inefficiency results in increased time consumption and hampers the overall performance of machine learning applications. Therefore, there is a pressing need for a specialized processor design that incorporates matrix multiplication as a core instruction and aims to decrease time consumption in machine learning.

**Introduction:**

Intellera is a groundbreaking project aimed at designing a RISC-V based processor with a customized instruction set architecture (ISA) that includes matrix multiplication instructions. The goal of Intellera is to address the performance bottleneck caused by conventional processors when executing matrix operations in machine learning algorithms. By enhancing the processor's capabilities and providing dedicated hardware acceleration for matrix Multiply-Accumulate (MAC) operations, Intellera aims to significantly reduce the time consumed in machine learning tasks.

**Mission:**

The mission of Intellera is to revolutionize the field of machine learning by developing a specialized hardware solution that empowers processors to execute matrix multiplication operations efficiently. By incorporating a customized instruction set with matrix multiplication support, Intellera aims to optimize the performance of machine learning algorithms, enabling faster and more efficient computations.

**Solution:**

Intellera proposes a novel approach to address the time consumption challenge in machine learning. The project focuses on designing a RISC-V based processor that features an extended instruction set architecture specifically tailored for matrix multiplication. By integrating dedicated hardware support for matrix MAC operations, Intellera can harness the parallel processing capabilities of the processor to accelerate matrix computations and reduce the overall execution time.

**Implementation:**

The implementation of the Intellera project involves multiple stages. Initially, we will design and develop a customized instruction set architecture (ISA) for the RISC-V processor, incorporating matrix multiplication instructions. Subsequently, we will integrate the matrix MAC accelerator into the processor's hardware design, ensuring seamless compatibility with the extended ISA. Finally, we will fabricate a system-on-chip (SoC) integrating the Intellera processor and try to run kernel.

**Tools:**

The Intellera project will leverage a range of tools and technologies. The design and development of the customized instruction set architecture will be facilitated by hardware description languages (HDLs) such as Verilog or VHDL. The implementation phase will involve FPGA-based prototyping and hardware synthesis tools to generate the final design for fabrication.

**Conclusion**:

Intellera is a groundbreaking project that aims to overcome the limitations of traditional processors in executing matrix multiplication tasks for machine learning. By designing a customized RISC-V processor with dedicated hardware support for matrix Multiply-Accumulate (MAC) operations, Intellera strives to reduce time consumption and enhance performance in machine learning applications. Successful implementation of Intellera could lead to future advancements in hardware-based acceleration for matrix computations, enabling faster and more efficient machine learning algorithms.